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D. Amendments to the Drawing.

There are no current amendments to the drawings.

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E. Remarks

Rejection of Claims 1-3, 5 and 21-22 Under 35 U.S.C. §102(b) based on U.S. Patent No. 5,780,910 (*Hashimoto et al.*).

Amended claim 1 is directed to a memory cell that includes a first node for storing a first potential, a second node for storing a second potential, transistor gate electrodes formed from a gate layer, and a capacitor having plates coupled between the first node and second node. A portion of one plate of the capacitor comprises a first interconnect wiring layer pattern, formed over the gate layer, that includes a plurality of conductive layers and that electrically interconnects circuit devices of the memory cell.

As is well established, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention.[1]

As emphasized above, amended claim 1 recites a "portion of one plate of the capacitor comprising a first interconnect wiring layer pattern". This first interconnect wiring layer pattern includes "a plurality of conductive layers" and "electrically interconnects circuit devices of the memory cell". Applicants do not believe that the cited reference shows or suggests such claim limitations.

Hashimoto et al. shows a static random access memory (SRAM) with a capacitor element having a stacked structure. The capacitors of *Hashimoto et al.* include a lower electrode separated from an upper electrode by a capacitor insulating film. However, in the various examples of *Hashimoto et al.*, the lower and upper electrodes are each different patterns of different single layer polycrystalline silicon (polysilicon) films:

> [A]s shown in FIGS. 12 and 13, *an* n-type polycrystalline silicon film... is patterned... to form the lower electrode 16 of the capacitor element C. (*Hashimoto et al.*, Col. 15, Line 66 to Col. 16, Line 3, emphasis added).

[1] Scripps Clinic & Research Found. v. Genetech Inc., 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991).

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> [A]s shown in FIGS. 16 and 17, ***the*** n-type polycrystalline silicon film... is patterned... to form the upper electrode 19 of the capacitor element C. (*Hashimoto et al.*, Col. 16, Lines 24-28, emphasis added).
>
> ***[T]he*** n-type polycrystalline silicon film... is patterned to form the lower electrode 41 of the capacitor element C, as shown in FIGS. 28 and 29. (*Hashimoto et al.*, Col. 19, Lines 23-26, emphasis added).
>
> [A]s shown in FIGS. 30 and 31... ***an*** n-type polycrystalline silicon film... is subsequently patterned to form the upper electrode 42 of the capacitor element C. (*Hashimoto et al.*, Col. 19, Lines 36-40, emphasis added).
>
> [A]s shown in FIGS. 55 and 56, ***the*** n-type polycrystalline silicon film... is patterned to form the lower electrode 61 of the capacitor element C. (*Hashimoto et al.*, Col. 27, Lines 45-48, emphasis added).
>
> [A]s shown in FIGS. 57 and 58... ***The*** n-type polycrystalline silicon film... is patterned to form the upper electrode 62 of the capacitor element C. (*Hashimoto et al.*, Col. 27, Lines 55-60, emphasis added).

Thus, *Hashimoto et al.* teaches electrodes formed by patterning single layers, and thus is not believed to show or suggest Applicants' claim 1 limitations of a "first interconnect wiring layer pattern" that includes "a plurality of conductive layers".

Applicants acknowledge that when viewed collectively, the lower/upper electrode pairs of *Hashimoto et al.* (i.e., 16/19, 41/42 and 62/62) do include multiple (two) polycrystalline films. However, such a combination of films cannot correspond to Applicants' "first interconnect wiring layer pattern", as the lower electrodes have an entirely different pattern than the upper electrodes. This is illustrated below in FIGS. 2(c) and 2(d) of *Hashimoto et al.*:

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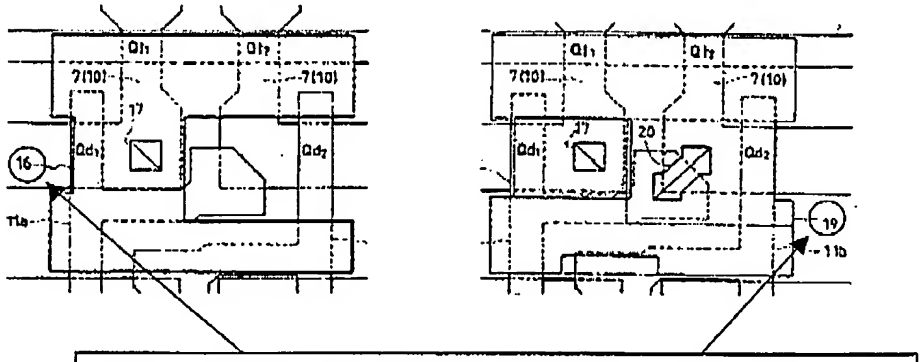

Lower capacitor electrode 16 is has different pattern and is formed from a different layer than upper electrode 19.

This same pattern difference is repeated for electrode pairs 41/42[2] and 61/62[3].

For these reasons, the cited reference is not believed to show or suggest all the limitations of claim 1.

Amended claim 5, which depends from claim 1, is believed to be separately patentable over the cited reference.

Amended claim 5 recites that the first interconnect wiring layer pattern includes a plurality of separate portions, each portion including a bottom conductive layer, a dielectric layer formed over the bottom conductive layer, and a top conductive layer formed over the dielectric layer. The bottom conductive layer forms at least a portion of a first plate of the capacitor.

As noted above in the comments for claim 1, *Hashimoto et al.* shows electrodes patterned from films. However, each such patterned electrode includes but one polycrystalline film. Therefore, because the reference provides teachings restricted to such single film patterns, Applicants believe the reference neither shows nor can be considered suggestive of Applicants' claim 5 wiring layer pattern, which includes not only a bottom and top conductive layers, but also a dielectric layer.

Accordingly, amended claim 5 is believed to include limitations not shown in or suggested by the cited reference.

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[2] See *Hashimoto et al.*, FIGS. 29 and 30.
[3] See *Hashimoto et al.*, FIGS. 56 and 58.

For all of these reasons, this ground for rejection is traversed.

Rejection of Claim 23 Under 35 U.S.C. §103(a) based on *Hashimoto et al.* in view of U.S. Patent No. 6,104,053 (*Nagai*).

The invention of claim 23 is directed to a memory cell that includes a first data storage node and a second data storage node. The memory cell also includes a capacitor comprising a first plate coupled to the first data storage node, a second plate coupled to the second data storage node, and a third plate separated from the first and second plates by a capacitor dielectric. The first and second plates comprise portions of an interconnect layer that electrically connects terminals of transistors of the memory cell to one another.

As indicated by the Federal Circuit, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

As emphasized above, Applicants' claim 23 recites "first and second plates" that "comprise portions of an interconnect layer". Such an arrangement is not believed to be shown or suggested by the cited reference.

Hashimoto et al. shows an SRAM cell with a capacitor having one electrode connected to one storage node, and another electrode connected to another storage node. However, as noted in the above comments for claim 1, the capacitor electrodes of *Hashimoto et al.* are formed from different polycrystalline films, thus such electrodes do not "comprise portions of an interconnect layer". Because all the examples of *Hashimoto et al.* show capacitor electrodes formed from different films, Applicants do not believe that the reference can be suggestive of Applicants' claim 23.

Nagai, the other cited reference, discloses capacitors employed in a logic circuit that can include three electrodes. However, in *Nagai*, each different electrode is formed from entirely different films. This is shown in FIG. 1 of *Nagai*:

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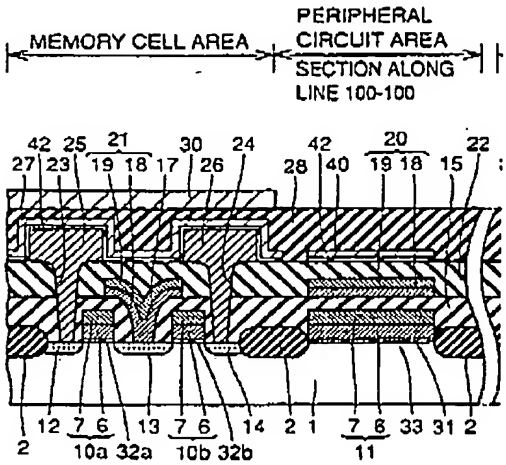

"The polysilicon film 6 and the tungsten silicide film 7 form a first electrode 11 of the capacitors... The polysilicon film 18 and the tungsten silicide film 19 form a second electrode 20 of the capacitors... A third electrode 40 of the capacitors is formed on the insulating film 42." (*Nagai*, Col. 11, Line 67 to Col. 12, Line 13).

Because the above teachings of *Nagai* show only capacitor electrodes of different layers, Applicants do not believe the reference can be suggestive of first and second plates "comprising portions of an interconnect layer", as recited in claim 23.

Accordingly, the cited combination of references is not believed to show or suggest all the limitations of claim 23. For this reason, Applicants do not believe that a prima facie case of obviousness has been established for this claim.

Equally well settled is the standard for patentability with respect to obviousness enunciated by the Supreme Court of the United States.

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined... As indicia of obviousness or nonobviousness, these inquires may have relevancy...[4]

Applicant believes that the above factors also illustrate how the invention of claim 23 is nonobvious in light of *Hashimoto et al.* in view of *Nagai*.

As noted from the above discussion, the cited references both fail to teach first and second capacitor plates "comprising an interconnect layer", and thus present substantial differences from the claim at issue.

[4] Graham v. John Deere, 383 U.S. 1 (1966). See also M.P.E.P. §2141.

Still further, the capacitor teachings of *Nagai* argued to show Applicants' capacitor plate arrangement are further removed from Applicants invention, as these teachings are directed to a peripheral circuit area (understood from FIG. 1 of *Nagai* shown above). Peripheral circuit areas are around a memory cell area, and hence not part of the memory cells of a device:

> In general, a semiconductor device such as a DRAM (dynamic random access memory) has a ***peripheral circuit area*** provided with a control logic circuit or the like ***around a memory cell area***. A capacitor is generally employed in the logic circuit of the peripheral circuit area. (*Nagai*, Col. 1, Lines 13-17, emphasis added).

In sharp contrast, Applicants' claim 23 is directed to a memory cell, and hence is applicable to a memory cell area, and not a peripheral area. Thus, the reference *Nagai* is believed to be very different from Applicants' claim 23 invention.

The level of ordinary skill in the art is believed to be reflected by both cited references showing capacitor electrodes consistently formed as parts of different films, and not "comprising an interconnect layer". No other evidence related to skill in the art has been presented.

Accordingly, the differences between Applicants' claim 23 and the cited reference, along with the skill in the art as reflected by the references, are believed to indicate the nonobviousness of Applicants' claim 23 invention.

For all of these reasons, this ground for rejection is traversed.

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Claims 1, 5, 6, 22 and 23 have been amended. Claim 23 was amended to correct a typographical error, and not in response to the cited art.

The present claims 1-3, 5-7, and 21-22 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

4/2/07

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